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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,526	06/23/2000	Joseph Herbst	108339-09031	1170

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EXAMINER	
LOGSDON, JOSEPH B	
ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 06/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/599,526	HERBST, JOSEPH	
	Examiner	Art Unit	
	Joe Logsdon	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,10,13,14,17 and 19-21* is/are rejected.

7)☒ Claim(s) *2-6, 8, 9, 11, 12, 15, 16, 18, and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Formal Drawings:

1. The formal drawings filed 01 April 2004 are accepted.

Claim Rejections—35 U.S.C. 103(a):

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi in view of Miller et al.

With regard to claim 1, Takahashi teaches a means for controlling *a buffer memory to store* the effective period of each of a predetermined number of scanning line periods per frame period selected from the plurality of scanning line periods per frame period of the first digital video signal *in response to a write clock signal* (claim 1). Takahashi fails to teach that the write clock signal is a glitchless fractional clock pulse. The specification does not provide a definition for "fractional," so any glitchless clock pulse is a glitchless fractional clock pulse. Miller et al. teaches the generation of a glitchless clock pulse and, therefore, the generation of a glitchless fractional clock pulse (column 1, lines 36-38). Miller et al. teaches that this arrangement prevents disruption of accurate communication (column 1, lines 26-35). It would have been obvious to one of ordinary skill in the art to modify the invention of Takahashi so that the write clock is a

glitchless fractional clock pulse because such an arrangement would prevent disruption of accurate communication.

4. Claims 10, 13, 14, 17, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in view of Takahashi.

With regard to claims 10, 13, 17, and 20, Miller et al. teaches receiving a clock signal in a logic circuit (CLKA or CLKB in Fig. 1); receiving a latch enable pulse in the logic circuit (NRESET in Fig. 1); generating a glitchless clock pulse and, therefore, a glitchless fractional clock pulse (the specification does not provide a definition for "fractional," so any glitchless clock pulse is a glitchless fractional clock pulse) (CLKOUT in Fig. 1; column 3, lines 7-10) in the logic circuit in response to the clock signal and the enable pulse (column 2, line 11 to column 3, line 18). Miller et al. teaches that this arrangement prevents disruption of accurate communication (column 1, lines 26-35). Miller et al. fails to teach transmitting a glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable period. Takahashi teaches a means for controlling *a buffer memory to store* the effective period of each of a predetermined number of scanning line periods per frame period selected from the plurality of scanning line periods per frame period of the first digital video signal *in response to a write clock signal* (claim 1). It would have been obvious to one of ordinary skill in the art to modify the invention of Miller et al. so that it teaches transmitting a write clock signal as a glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable period because such an arrangement would prevent

disruption of accurate communication during the times when data are transferred to the latches for storage.

With regard to claim 14 and 21, Takahashi fails to teach that the at least one storage element comprises at least one latch. It would have been obvious to one of ordinary skill in the art to modify the invention of Takahashi so that the storage element comprises a latch because a latch could be used to store data.

With regard to claim 19, Takahashi fails to teach a memory management unit for controlling the storage of data in the at least one storage element. It would have been obvious to one of ordinary skill in the art to modify the teaching of Takahashi so that it teaches a memory management unit for controlling the storage of data in the at least one storage element because such an arrangement would enable the process of storing data to be controlled.

Reasons for Allowance:

5. The prior art does not teach or fairly suggest the method for storing data comprising the steps of receiving a data storage enable signal; receiving a system clock signal; generating a glitchless fractional clock pulse, wherein the period of the pulse is less than the period of the system clock signal; and outputting the glitchless fractional clock pulse, as specified in dependent claim 2.

The prior art does not teach or fairly suggest the method comprising the steps of receiving a clock signal, wherein the clock signal has a plurality of equally spaced and timed pulses; receiving a data storage enable signal; and generating the glitchless fractional pulse on an

output of the circuit in response to the data storage enable signa, wherein the duration of the glitchless fractional clock pulse is less than the duration of the clock signal pulse and is positioned between the rising edge and the falling edge of a corresponding clock pulse, as specified in dependent claim 6.

The prior art does not teach or fairly suggest the method wherein the generating step of claim 1 comprises generating a glitchless fractional clock pulse having a period less than a period of the system core clock pulse, as specified in dependent claim 8.

The prior art does not teach or fairly suggest the method wherein the generating step further comprises generating the glitchless fractional clock pulse is generated between a rising edge and a falling edge of the system core clock pulse, as specified in dependent claim 9.

The prior art does not teach or fairly suggest the method of claim 10 wherein the step of generating a glitchless fractional clock pulse further comprises the steps of receiving a latch enable signal at a first flip flop; receiving a clock signal at a second input of a second flip flop and at the second input of the first flip flop; receiving an output of the first flip flop at a first input of the second flip flop and a first input of an AND gate; receiving an output of the second flip flop at a second inverted input of the AND gate; and generating the glitchless fractional clock pulse at an output of the AND gate, as specified in dependent claim 11.

The prior art does not teach or fairly suggest the apparatus of claim 13, wherein the logic circuit further comprises a first flip flop having a first CLK input, a first dat input, and a first output; a second flip flop having a second CLK input, a second data input, and a second output; and an AND gate having a first input, a second inverted input, and an output; wherein the first output of the first flip flop is connected to the second data input of the second flip flop and the

first input of the AND gate, the second output of the second flip flop is connected to the second inverted input of the AND gate, a system clock pulse is connected to the first CLK input and the second CLK input of the first and second flip flops, a latch enable pulse is received on the first data input of the first flip flop, and a glitchless fractional clock pulse is generated on the output of the AND gate and transmitted to the storage enable input on the storage element, as specified in dependent claim 15.

The prior art does not teach or fairly suggest the apparatus of claim 13, wherein the glitchless fractional clock pulse generated at the logic output of the AND gate further comprises a glitchless fractional clock pulse having a width that is less than the width of a system clock pulse and positioned between a rising edge and a falling edge of the system cloak pulse, as specified in dependent claim 16.

The prior art does not teach or fairly suggest the method of claim 17, wherein the network switch further comprises a communication channel in connection with the at least one data port interface for communicating data in the network switch, as specified in dependent claim 18.

The prior art does not teach or fairly suggest the apparatus of claim 20, wherein the pulse generating means further comprises a first flip flop having a first CLK input, a circuit enable input, and a first output; a second flip flop having a second clock input in connection with the first clock input of the first flip flop, a data input in connection with the first output of the first flip flop, and a second output; and an AND gate having a first input in connection with the first output of the first flip flop, a second inverted input in connection with the second output of the second flip flop, and an output, wherein the glitchless fractional clock pulse is generated on the

output of the AND gate upon receiving an enable pulse at the circuit enable input, as specified in dependent claim 22.

Response to Arguments:

6. Applicant argues that the definition of fractional glitchless clock pulse is limited to the description provided in the specification. Applicant quotes a portion of the specification, which Applicant claims defines "fractional" as used in "glitchless fractional clock pulse." But the quoted portion only discusses the meaning of "glitchless fractional clock pulse"; the quoted portion fails to describe how a "glitchless fractional clock pulse" differs from a "glitchless clock pulse." Similarly, Applicant refers to Fig. 32; but Fig. 32 does not reveal the meaning of "fractional."

With regard to claim 17, Applicant argues that the specification discusses the elements and functioning of a switch. But Examiner cannot read the specification into the claims. If Applicant intends that the meaning be limited to that provided in the specification, then Applicant should claim it as such.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joe Logsdon whose telephone number is (703) 305-2419. The examiner can normally be reached on Monday through Friday from 10:00 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on 703-305-4744. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joe Logsdon

Patent Examiner

Friday, June 18, 2004

HASSAN KIZOU
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